Remarks

Reconsideration and allowance of the subject patent application are respectfully requested.

A Listing of Claims is provided for the Examiner's convenient reference.

Applicants acknowledge with appreciation the indication that claims 13, 15, 24, 26, 36, 38, 41, 42 and 52 contain allowable subject matter.

Claims 1-7, 14, 16-18, 25, 27-30, 37, 39, 43-46, 53 and 54 were rejected under 35 U.S.C. Section 103(a) as allegedly being made "obvious" by Chin et al. (U.S. Patent No. 6,202,101) in view of Harriman et al. (U.S. Patent No. 6,092,158).

Chin et al. discloses a memory controller 44 "embodied within interface controller 14, as shown in FIG. 2." Chin et al., col. 8, lines 25-26. Chin et al. does not disclose or suggest that memory controller 44 includes the features set forth in the pending claims and indeed there is no assertion by the Examiner to this effect. Instead, the Examiner contends that the entirety of interface controller 14 (which includes separate PCI, processor and memory controllers) is a memory controller. On its face, this contention is plainly inconsistent with the disclosure of Chin et al., which shows and describes a memory controller as part of the interface controller.

In response to Applicant's prior comments on this issue, the Examiner responds as follows:

> In reply, the Examiner points out that the Applicants' own disclosure was merely used to define what is meant by Applicants' claimed "memory controller". Since Applicants' own disclosure defines the claimed "memory controller" in the same manner as the "interface controller" of Chin (US006202101B1), the "interface controller" of Chin is considered to be equivalent to the claimed "memory controller".

This position is legally and factually wrong.

First, Applicant respectfully requests that the Examiner identify the legal basis for using Applicant's disclosure to "define what is meant" by the claimed memory controller. The various claims define what is meant by the memory controller and the Examiner's attempts to compare the prior art to the example embodiments disclosed in the specification and to limit the claims to these example embodiments are legally improper.

Second, Applicant's disclosure clearly does not define a memory controller "in the same manner" as the interface controller of Chin et al. For example, Figure 3 and the accompanying

description of the subject patent application show an example graphics and audio processor that includes a processor interface 150, a memory interface/controller 152 and a peripheral controller 162. Thus, the examples in Applicant's disclosure show the memory interface/controller 152 as being separate from the processor interface 150 and peripheral controller 162. Applicant's disclosure does not use the term "memory controller" to collectively refer to processor interface 150, memory interface/controller 152, and peripheral controller 162. Consequently, contrary to the Examiner's assertions, Applicant's disclosure supports Applicant's position that the Examiner improperly uses "memory controller" to collectively refer to the separate PCI, processor and memory controllers in Chin et al.

Applicant provides the following additional comments in response to certain statements contained in the Advisory Action dated April 4, 2007.

In response to Applicant's contention that queue 50c is not a request queue, the Advisory Action contends:

> In reply, the Examiner points out that Chin discloses that a bus interface unit dispatches memory request cycles to respective target devices (Col. 1, lines 10-15). Figure 2 is a diagram of the bus interface unit (Col. 6, lines 50-54), and shows that cycles are passed between controllers using queues which link respective controllers (Col. 8, lines 23-44). Since cycles are passed using the queues, and these cycles are memory request cycles, the queues are considered to store information indicative of a request for main memory access, as recited in Claim 1.

While Chin et al. describes passing cycles between the controllers using queues, there is no basis for the Examiner's contention that cycles passed using queue 50c are memory request cycles. The Examiner's position is belied by Figure 2 in which the arrow between memory controller 44 and queue 50c points toward queue 50c and by the very col. 8 description referenced by the Examiner which states that 50c is a "memory-to-processor" queue. Similarly, queues 50d and 50h store data read from the memory, not requests for such data. The Examiner's contentions to the contrary in the Advisory Action are simply inconsistent with Chin et al.'s disclosure.

In summary, Chin et al. does not disclose or suggest memory controllers or methods as recited in the pending claims. Specifically, Chin et al. does not describe the memory controller 44 disclosed therein as including or providing the claimed features. Moreover, even if the entirety of the interface controller 14 disclosed in Chin et al. is erroneously viewed as a memory controller as suggested by the Examiner, this controller does not include or provide the claimed

features for the reasons set forth in the responses of March 15, 2007 and September 22, 2006, which responses are incorporated herein in their entirety.

As previously discussed, Harriman et al. does not remedy the deficiencies of Chin et al. with respect to the claimed buffer memories, multiple resource buffer memory and/or control circuit. As such, even assuming for the sake of argument that Harriman et al.'s technique of reducing turnaround is viewed as reducing the switching frequency of main memory read and write operations and this technique were forcibly combined with Chin et al., the subject matter of claim 1, for example, could still not possibly result.

For at least these reasons, Applicants respectfully submit that the subject matter of claim 1 and its dependent claims 2-7 and 14 would not have been made obvious by the proposed combination of Chin et al. and Harriman et al.

These dependent claims contain features that provide additional bases for patentability.

By way of example, claim 14 requires that a resource that is writing to main memory generates a flush signal for initiating the flushing of that resource's write request queue. The office action contends that the "de-queuing" described at col. 13, lines 1-11 of Chin et al. discloses this feature. However, this de-queuing is for queue 50c, which contains data whose source is the memory and whose destination is the processor. This queue is not a write request queue and there is no disclosure or suggestion in Chin et al. of initiating the flushing of a resource's write request queue when that resource is writing to main memory. For this additional and independent reason, claim 14 is believed to distinguish over the proposed combination of Chin et al. and Harriman et al.

Claim 16 is for a memory controller comprising a main processor related interface including read and write request queues; a first resource related interface including read and write request queues; a second resource related interface including read and write queues; and a multiple resource write request queue. Among other things, this rejection is premised in part on the identification of queue 50c as a "read request queue". As discussed above, queue 50c is not a read request queue and thus the rejection fails to identify in Chin et al. a read request queue for a main processor related interface.

Harriman et al. does not remedy the deficiencies of Chin et al. with respect to these features and, consequently, the proposed combination of these documents is deficient in this regard with respect to claim 16 and its dependent claims 17, 18 and 25.

These dependent claims contain features that provide additional bases for patentability.

By way of example without limitation, claim 25 requires that a resource that is writing to main memory generates a flush signal for initiating the flushing of that resource's write request queue. The office action contends that the "de-queuing" described at col. 13, lines 1-11 of Chin et al. discloses this feature. However, as noted above in the discussion of claim 14, this de-queuing operation is for queue 50c, which contains data whose source is the memory and whose destination is the processor. This queue is not a write request queue and there is no disclosure or suggestion in Chin et al. of initiating the flushing of a resource's write request queue when that resource is writing to main memory. For this additional and independent reason, claim 25 is believed to distinguish over the proposed combination of Chin et al. and Harriman et al.

With respect to claim 27, queues 50d and 50h are identified by the Examiner as request queues. However, these queues are in fact a memory-to-PCI queue and a memory-to-AGP queue, respectively, and, as mentioned above, store data read from the memory, not requests for such data.

Consequently, the proposed combination of Chin et al. and Harriman et al. would not have resulted in the subject matter of claim 27 or its dependent claims 28-30, 37, 39, 40, 43-46 and 53.

These dependent claims contain features that provide additional bases for patentability.

By way of example without limitation, claim 37 requires that a resource that is writing to main memory generates a flush signal for initiating the flushing of that resource's write request queue. The office action contends that the "de-queuing" described at col. 13, lines 1-11 of Chin et al. discloses this feature. However, as noted above in the discussion of claim 14, this de-queuing is with respect to queue 50c, which contains data whose source is the memory and whose destination is the processor. This queue is not a write request queue and there is no disclosure or suggestion in Chin et al. of initiating the flushing of a resource's write request queue when that resource is writing to main memory. For this additional and independent reason, claim 37 is believed to distinguish over the proposed combination of Chin et al. and Harriman et al.

Claim 40 is for a method of controlling access to a main memory which requires generating a write queue flush signal by a first resource to initiate copying information in the first resource write request queue to main memory and flushing the first resource write request queue. Among other things, the col. 13, lines 1-11 disclosure of Chin et al. referenced in the office action in connection with these features does not describe or suggest generating a flush

signal or flushing a write request queue. The first lines of this disclosure describe operations involving data read from the memory and stored in queue 50c. There is nothing here about write queues or the flushing of such queues. The last few lines of this disclosure state: "If the memory request is a write request, then the address will be held in the P2M queue (queue 50a) until that request's entry number matches the current in-order queue entry number." This description relates to write requests, but simply describes how long an address is held in a queue. There is nothing about the flushing of a write request queue. Consequently, claim 40 and its dependent claims 43-51 are not made obvious by the proposed combination of Chin et al. and Harriman et al.

Like claim 1, claim 54 similarly calls for buffer memories, a multiple resource buffer and control circuit. Consequently, Applicants respectfully submit that the subject matter of claim 54 would not have been made obvious by the proposed combination of Chin et al. and Harriman et al.

Claims 8-12, 19-23, 31-35 and 47-51 were rejected under 35 U.S.C. Section 103(a) as allegedly being "obvious" over the proposed Chin et al-Harriman et al. combination, in view of Jeddeloh et al. (U.S. Patent No. 6,330,647). Applicants respectfully traverse this rejection.

Jeddeloh et al. was applied in connection with its alleged disclosure of an arbiter and control registers. However, even assuming that such features were somehow shown to be properly combinable with the result of the Chin et al.-Harriman et al. combination, Jeddeloh et al. does not remedy the deficiencies of Chin et al. and Harriman et al. with respect to claims 1, 16, 27 and 40, from which claims 8-12, 19-23, 31-35 and 47-51 depend.

The pending claims are believed to be in condition for allowance and favorable office action is respectfully requested.

Respectfully submitted,

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